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Information can also be obtained from the Acorn Support Information Database (SID). This is an on-line viewdata system available to registered SID users. Initially, access SID on Cambridge (0223) 243642: this will allow you to inspect the system and use a response frame for registration.

Within this publication, the term 'BBC' is used as an abbreviation for 'British Broadcasting Corporation'.

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Contents

About this manual

The A3000 Technical Reference Manual is intended as a hardware reference manual for the A3000 computer, supplementing the basic information given on system hardware in the A3000 Welcome Guide, supplied with the computer.

It will be of interest to system integrators, software developers and those developing expansion cards for the A3000 computer.

The A3000 operating system, RISC OS, is covered at the user level in the User Guide supplied with the computer. Programmers and users requiring a greater depth of information about RISC OS will need the RISC OS Programmer's Reference Manual, available from Acorn authorised dealers.

Full details on the Acorn ARM chip set used in the A3000 are given in the 'VL86C010 RISC Family Data Manual' available from VLSI Technology Incorporated, of 486-488 Midsummer Blvd., Saxon Gate West, Central Milton Keynes, MK9 2EQ.

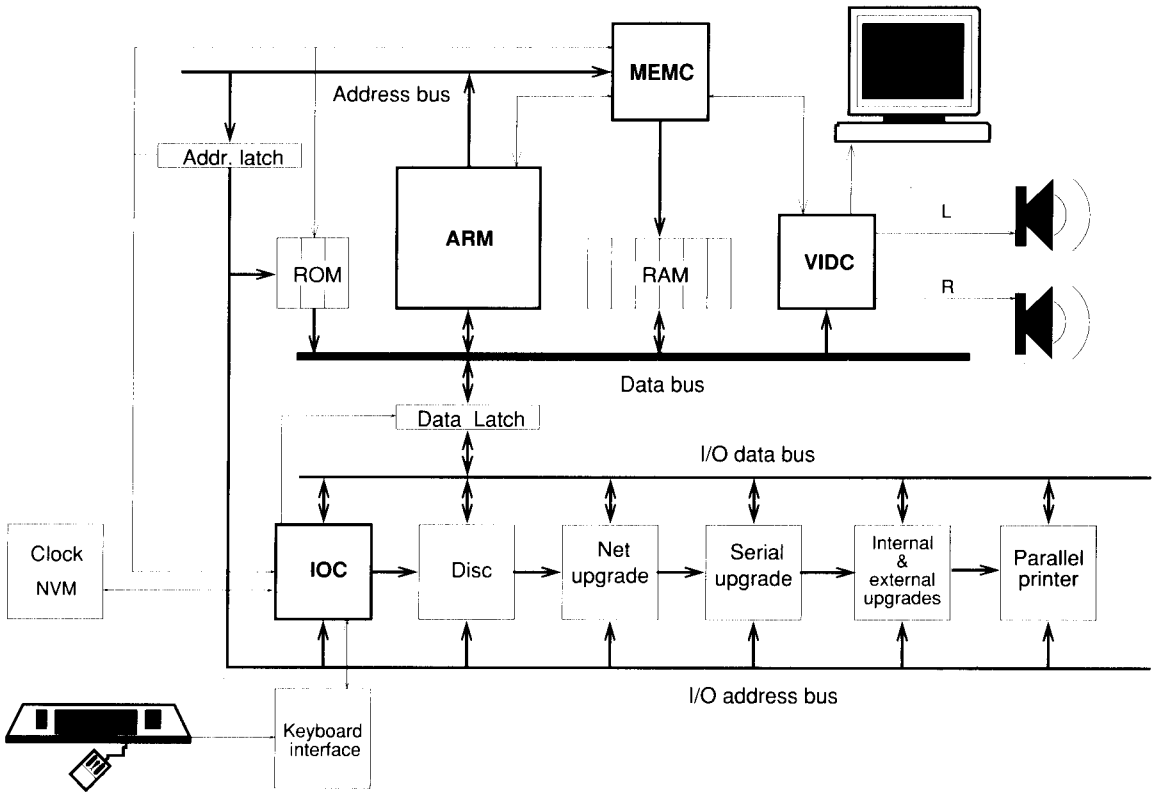
The Manual describes A3000s with Issue 1 PCBs. The differences between Issue A and Issue 1 boards, together with the changes made during the production of Issue A boards, are also included, starting on page 23.

System Description

Introduction

The A3000 computer is built around the ARM chip set, comprising the Acorn Risc Machine (ARM) itself, the Memory Controller (MEMC), Video Controller (VIDC) and Input Output Controller (IOC).

A block diagram of the A3000 is shown below:



General

The ARM IC is a pipelined, 32-bit reduced instruction set microprocessor which accepts instructions and manipulates data via a high speed 32-bit data bus and 26-bit address bus, giving a 64 MByte uniform address space. The ARM supports virtual memory systems using a simple but powerful instruction set with good high-level language compiler support.

MEMC acts as the interface between the ARM, VIDC, IOC, ROM (Read-Only Memory) and DRAM (Dynamic RAM) devices, providing all the critical system timing signals, including processor clocks.

1 or 2 MByte of DRAM is connected to MEMC which provides all signals and refresh operations. A Logical to Physical Translator maps the Physical Memory into a 32 MByte Logical address space (with three levels of protection) allowing Virtual Memory and Multi-Tasking operations to be implemented. Fast page mode DRAM accesses are used to maximise memory bandwidth. VIDC requests data from the RAM when required and buffers it in one of three FIFOs before using it. Data is requested in blocks of four 32-bit words, allowing efficient use of paged-mode DRAM without locking the system data bus for long periods.

MEMC supports Direct Memory Access (DMA) operations with a set of programmable DMA Address Generators which provide a circular buffer for Video data, a linear buffer for Cursor data and a double buffer for Sound data.

IOC controls the I/O bus and expansion cards, and provides basic functions such as the keyboard interface, system timers, interrupt masks and control registers. It supports a number of different peripheral cycles and all I/O accesses are memory mapped.

VIDC takes video data from memory under DMA control, serialises it and passes it through a colour

look-up palette and converts it to analogue signals for driving the CRT guns. VIDC also controls all the display timing parameters and controls the position and pattern of the cursor sprite. In addition, it incorporates an exponential Digital to Analogue Converter (DAC) and stereo image table for the generation of high-quality sound from data in the DRAM.

VIDC is a highly programmable device, offering a very wide choice of display formats. The colour look-up palette which drives the three on-chip DACs is 13 bits wide, offering a choice from 4096 colours or an external video source.

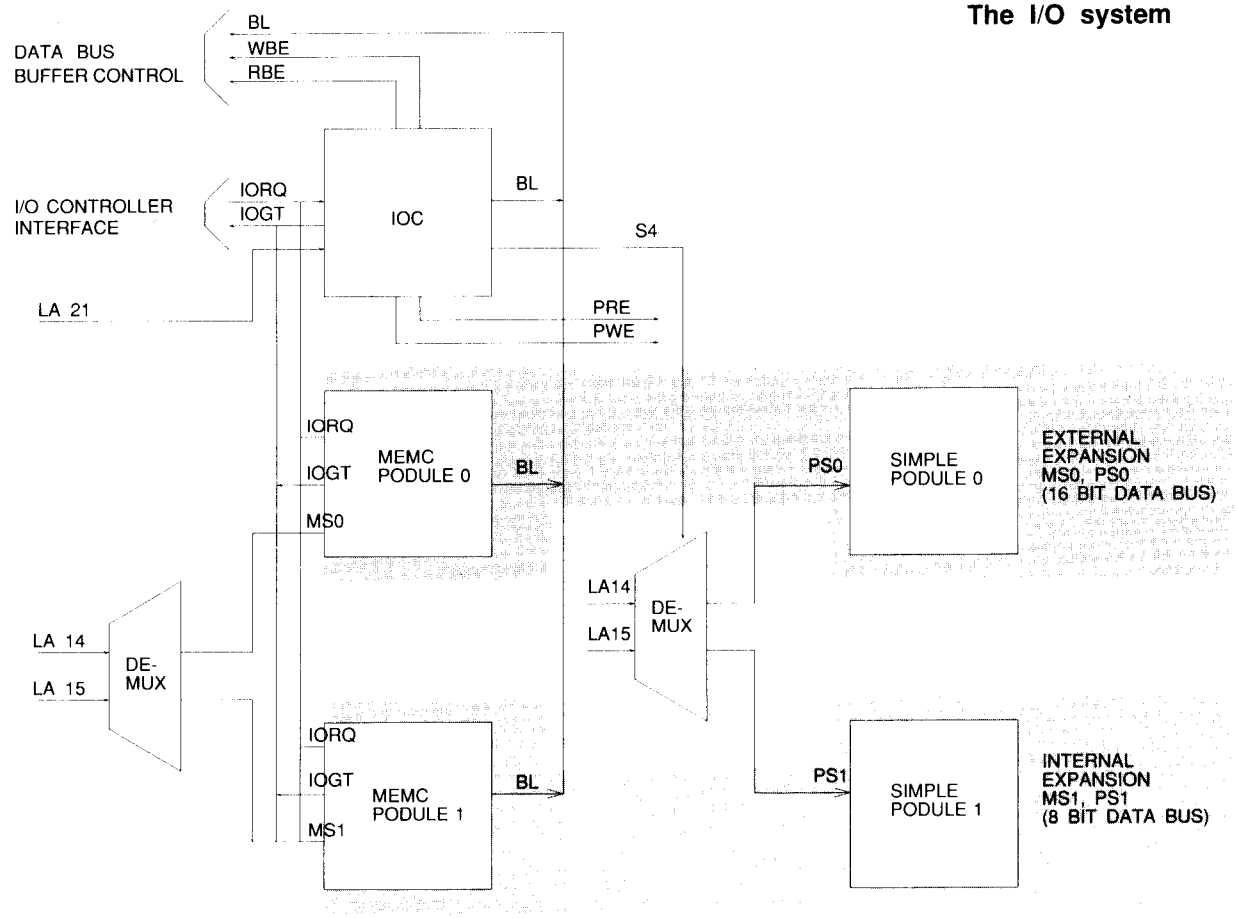
The cursor sprite is 32 pixels wide and any number of rasters high. Three simultaneous colours (again from a choice of 4096) are supported and any pixel can be defined as transparent, making possible cursors of many shapes. It can be positioned anywhere on the screen. The sound system implemented on the device can support up to eight channels, each with a separate stereo position.

The I/O system

The I/O system is controlled by IOC and MEMC. The I/O bus supports all the internal peripherals and the expansion cards. Details of the expansion bus can be found in the Chapter entitled 'A3000 Expansion'.

This section is intended to give the reader a general understanding of the A3000 I/O system and should not be used to program the I/O system directly. The implementation details are liable to change at any time and only the published software interfaces should be used to manipulate the I/O system. Future systems may have a different implementation of the I/O system, and in particular the addresses (and number) of expansion card locations may move. For this reason, and to ensure that any device may be plugged into any slot, all driver code for expansion cards must be relocatable. References to the direct expansion card addresses should never be used. It is up to the machine operating system, in conjunction with the expansion card ID, to determine the address at which an expansion card should be accessed. To this extent, some of the following sections are for background information only.

The I/O system



System architecture

The I/O system (which includes expansion card devices) consists of a 16-bit data bus (BD[0:15]), a buffered address bus (LA[2:21]), and various control and timing signals. The I/O data bus is independent of the main 32-bit system data bus, being separated from it by bidirectional latches and buffers. In this way the I/O data bus can run at much slower speeds than the main system bus to cater for slower peripheral devices. The latches between the two buses, and hence the I/O bus timing, are controlled by the I/O controller, IOC. IOC caters for four different cycle speeds (slow, medium, fast and synchronous).

A typical A3000 I/O system is shown in the diagram on the previous page. For clarity, the data and address buses are omitted from this diagram.

System memory map

The system memory map is defined by MEMC, and is shown below. Note that all system components, including I/O devices, are memory mapped.

I/O space memory map

This IOC-controlled space has allocation for simple expansion cards and MEMC expansion cards.

Data bus mapping

The I/O data bus is 16 bits wide (eight bits wide for internal expansion cards). Bytewide accesses are used for 8-bit peripherals. The I/O data bus (BD[0:15]) connects to the main system data bus (D[0:31]) via a set of bidirectional data latches.

The mapping of the BD[0:15] bus onto the D[0:31] bus is as follows:

During a WRITE (ie ARM to peripheral) D[16:31] is mapped toBD[0:15].

During a READ (ie peripheral to ARM) BD[0:15] is mapped to D[0:15].

Byte accesses

To access bytewide expansion cards, byte instructions are used. A byte store instruction will place the written byte on all four bytes of the word, and will therefore correctly place the desired value on the lowest byte of the I/O bus. A byte or word load may be used to read a bytewide expansion card into the lowest byte of an ARM register.

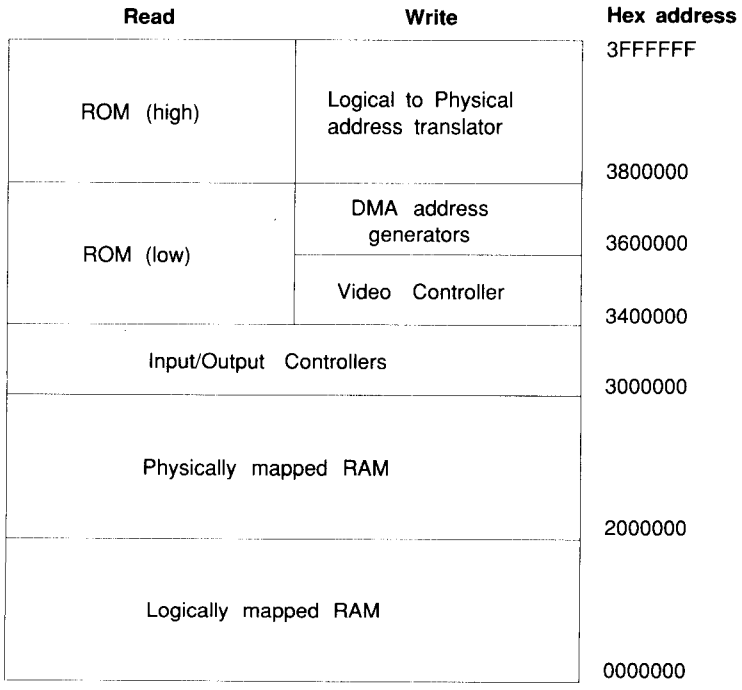
Half-word accesses

To access a 16-bit wide expansion card, half-word instructions are used. When storing, the half-word is placed on the upper 16 bits, D[16:31]. To maintain upwards compatibility with future machines, half-word stores replicate the written data on the lower half-word, D[0:15]. When reading, the upper 16 bits are undefined.

Expansion card identification

It is important that the system is able to identify what expansion cards (if any) are present, and where they are. This is done by reading the Podule (expansion card) Identification (PI) byte, or bytes, from the Podule Identification Field.

System memory map



Interrupts

The I/O system generates two independent interrupt requests, IRQ and FIQ. Interrupt requests can be caused by events internal to IOC or by external events on the interrupt or control port input pins.

The interrupts are controlled by four types of register:

- status
- mask
- request
- clear

The status registers reflect the current state of the various interrupt sources. The mask registers determine which sources may generate an interrupt. The request registers are the logical AND of the status and mask registers and indicate which sources are generating interrupt requests to the processor. The clear register allows clearing of interrupt requests where appropriate. The mask registers are undefined after power up.

The IRQ events are split into two sets of registers, A and B. There is no priority encoding of the sources.

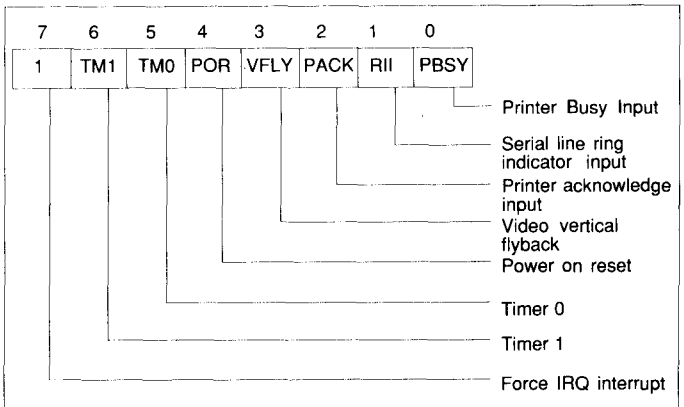
Internal Interrupt Events

- Timer interrupts TM[0:1]
- Power-on reset POR
- Keyboard Rx data available SRx
- Keyboard Tx data register empty STx
- Force interrupts 1.

External Interrupt Events

- IRQ active low inputs IL[0:7] wired as (0-7 respectively) PFIQ, SIRQ, SLC1, not used, DCIRQ, PIRQ, PBSY and RII.
- IRQ falling-edge input IF wired as PACK
- IRQ rising-edge iput IR wired as VFLY
- FIQ active high inputs FII[0:1] wired as FFDQ and FFIQ
- FIQ active low input FL wired as EFIQ
- Control port inputs C[3:5].

IRQ status A

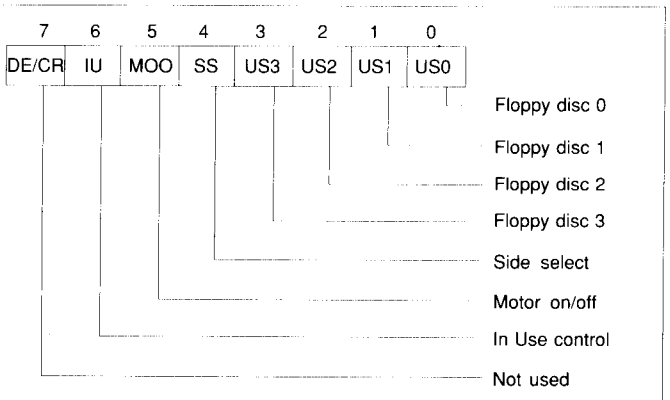


Bit	Name	Function
0	PBSY	This bit indicates that the printer is busy.
1	RII	This bit indicates that a Ringing Indication has been detected by the serial line interface.
2	Printer Ack	This bit indicates that a printer acknowledgement bit has been received.
3	Vertl Flyback	This bit indicates that a vertical flyback has commenced.
4	Power-on reset	This bit indicates that a power-on reset has occurred.
[5:6]	Timer 0 and Timer 1 events	These bits indicate that events have occurred. Note: latched interrupt.
7	Force	This bit is used to force an IRQ request. It is usually owned by the FIQ owner and is used to downgrade FIQ requests into IRQs.

I/O programming details

External latch A

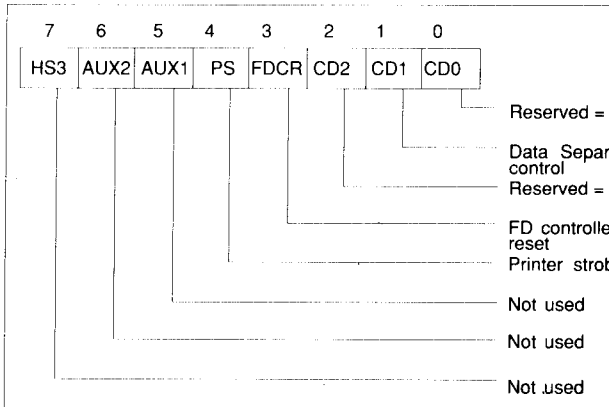
External latch A is a write only latch used to control parts of the floppy disc sub-system:



Bit	Name	Function
0-3	Floppy disc sel.	These bits select the floppy disc drive 0 through 3 when written LOW. Only one bit should be LOW at any one time.
4	Side select	This controls the side select line of the floppy disc interface. 0 = Side 1 (upper) 1 = Side 0 (lower)
5	Floppy motor	This bit controls the floppy disc on/off control motor line. Its exact use depends on the type of drive.
6	In Use	This bit controls the IN USE line of the floppy disc. Its exact use depends on the type of drive.
7		Not used.

External latch B

External Latch B is a write only register shared between several users who must maintain a consistent RAM copy. Updates must be made with IRQ disabled.

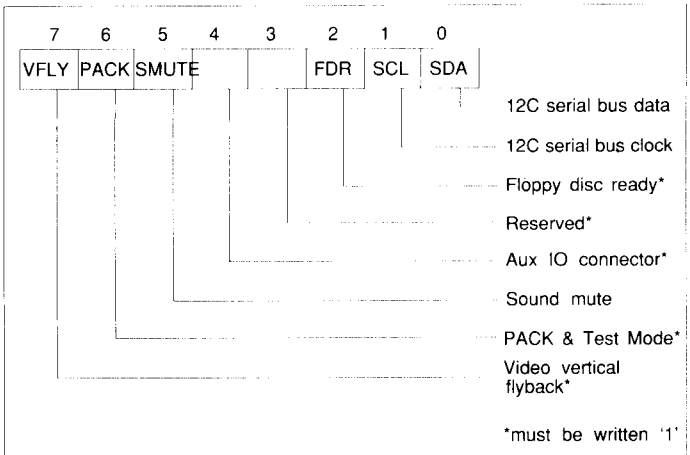


Bit	Name	Function
0-2		CD[0:2] should be programmed CD[0.2] LOW for future compatibility. CD[1] controls the floppy disc data separator format. CD[1] = 0 Double Density CD[1] = 1 Single Density
Bit 3	FDCR	This controls the floppy disc controler reset line. When programmed LOW, the controller is RESET.
Bit 4	Printer Strobe	This is used to indicate valid data on the printer outputs. It should be set HIGH when valid data has been written to the printer port and LOW after about 5 µs.
Bit [5:6]	AUX [1:2]	Not used.
Bit 7	HS3	Not used.

Control port

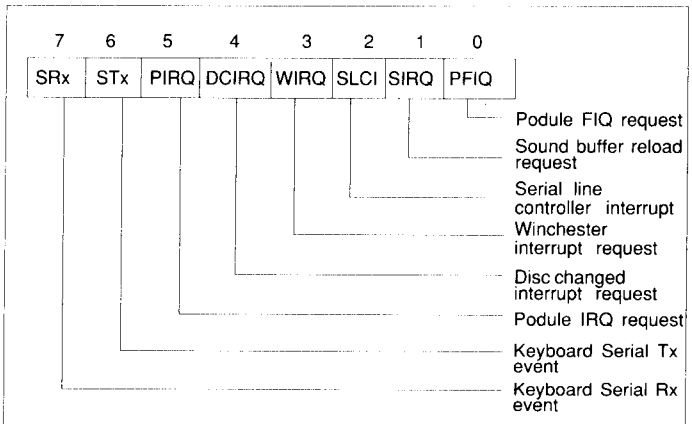
The control register allows the external control pins C[0:5] to be read and written and the status of the PACK and VFLY inputs to be inspected. The C[0:5] bits manipulate the C[0:5] I/O port. When read, they reflect the current state of these pins. When written LOW the output pin is driven LOW. These outputs are open-drain, and if programmed HIGH the pin is undriven and may be treated as an input.

On reset all bits in the control register are set to 1.



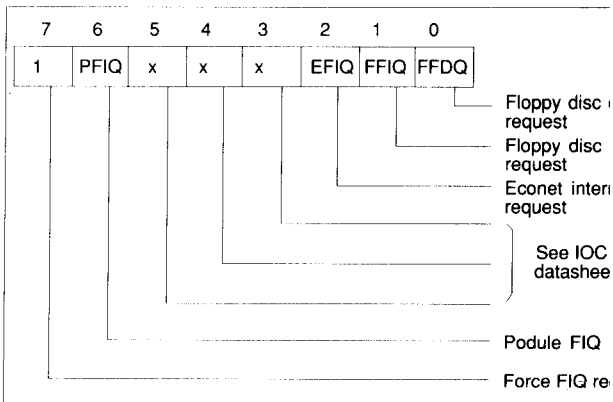
Bit	Name	Function
C[7]	VFLYBK and Test Mode	Allows the state of the (VFLYBK) signal to be inspected. This bit will be read HIGH during vertical flyback and LOW during display. See VIDC datasheet for details. This bit MUST be programmed HIGH to select normal operation of the chip.
C[6]	PACK & Test Mode	Allows the state of the parallel printer acknowledge input to be inspected. This bit MUST be programmed HIGH to select normal operation of the chip.
C[5]	SMUTE	This controls the muting of the internal speaker. It is programmed HIGH to mute the speaker and LOW to enable it. The speaker is muted on reset.
C[4]		Available on the Auxiliary I/O connector.
C[3]		Reserved and should be programmed HIGH.
C[2]	READY	Used as the floppy disc (READY) input and must be programmed HIGH.
C[1:0]	SDA, SCL the I2C bus	The C[0:1] pins are used to implement the bi-directional serial I2C bus to which the Real Time Clock and battery-backed RAM are connected.

IRQ status B



Bit	Name	Function
0	Podule FIQ req	This bit indicates that a Podule FIQ request has been received. It should usually be masked OFF.
1	Snd buffr swap	This bit indicates that the MEMC sound buffer pointer has been relocated.
2	Serial line ctrlr	This bit indicates that 65C51 serial line controller interrupt has occurred.
3	H disc interrupt	This bit indicates that a hard disc interrupt has occurred.
4	Disc changed Interrupt	This bit indicates that the floppy disc has been removed.
5	Pod. interr req	This bit indicates that a Podule IRQ request has occurred.
6	Keyb Tx event	This bit indicates that the keyboard transmit register is empty and may be reloaded.
7	Keybd Rx event	This bit indicates that the keyboard reception register is full and may be read.

Interrupt status FIQ



Bit	Name	Function
0	Floppy disc data request	This bit indicates that a floppy disc Data Request has occurred.
1	Floppy disc interrupt request	This bit indicates that a floppy disc Interrupt Request has occurred.
2	Econet Interrupt request	This bit indicates that an Econet Interrupt Request has occurred.
3-5	C[3:5]	See IOC data sheet for details.
6	Podule FIQ req	This bit indicates that a podule FIQ Request has occurred.
7	Force	This bit allows an FIQ Interrupt Request to be generated.

The keyboard and mouse

The keyboard and mouse connection to the ARM is made via a keyboard controller and a serial link to the IOC. The ARM reads and writes to the KART registers in the IOC. The protocol is essentially half duplex, so in normal operation the keyboard controller will not send a second byte until it has received an Ack. The only exception to this is during the reset protocol used to synchronise the handshaking, where each side is expecting specific responses from the other, and will not respond further until it has these.

In addition to this simple handshaking system, the keyboard controller will not send mouse data unless specifically allowed to, as indicated by Ack Mouse, which allows the transmission of one set of accumulated mouse coordinate changes, or the next move made by the mouse. While it is not allowed to send mouse changes, the keyboard controller will buffer mouse changes.

A similar handshake exists on key changes, transmitted as key up and key down, and enabled by Ack Scan. At the end of a keyboard packet (two bytes) the operating system will perform an Ack Scan as there is no protocol for re-enabling later. Mouse data may be requested later by means of Request Mouse Position (RQMP).

Key codes

The keyboard controller identifies each key by its row and column address in the keyboard matrix. Row and column codes are appended to the key up or down prefix to form the complete key code.

For example, Q key down – the complete row code is 11000010 (&C2) and the column code is 11000111 (&C7).

Note: Eight keys have N key roll over. The operating system is responsible for implementing two-key rollover, therefore the keyboard controller transmits all key changes (when enabled). The keyboard controller does not operate any auto-repeat; only one down code is sent, at the start of the key down period.

Data protocol

Data transmissions from the keyboard are either one or two bytes in length. Each byte sent by the keyboard controller is individually acknowledged. The keyboard controller will not transmit a byte until the previous byte has been acknowledged, unless it is the HRST (HardReSeT) code indicating that a power on or user reset occurred or that a protocol error occurred; see paragraph below.

Reset protocol

The keyboard controller restarts when it receives an HRST code from the ARM. To initiate a restart the keyboard controller sends an HRST code to the ARM, which will then send back HRST to command a restart.

The keyboard controller sends HRST to the ARM if:

- A power-on reset occurs
- A user reset occurs
- A protocol error is detected.

After sending HRST, the keyboard controller waits for an HRST code. Any non-HRST code received causes

```
START reset
ONerror Send HRST code to ARM then wait for code from ARM.
IF code = HRST THEN  restart  ELSE  error
ONrestart   clear mouse position counters
            set mouse mode to data only in response to an RMPS request.
            stop key matrix scanning and set key flags to up
            send HRST code to ARM
Wait for next code
IF code = RAK1 THEN send RAK1 to ARM    ELSE   error
Wait for next code
IF code = RAK2 THEN send RAK2 to ARM    ELSE   error
Wait for next code
IF code = SMAK THEN mouse mode to send if not zero and enable key scan
ELSE  IF code = SACK THEN enable key scanning
ELSE  IF code = MACK THEN set mouse mode to send when not zero
ELSE  IF code = NACK THEN  do nothing   ELSE  error
END reset

Reset sequencing
Direction   Code        Expected    Action on   Action on   Action if
                        reply       wrong reply timeout     unexpected
                                    (Sender)    (Sender)    (Receiver)

ARM -> Kb   Hard reset  Hard reset  Resend      Resend      Hard reset
Kb  -> ARM  Hard reset  Reset Ack 1 Resend      Nothing     Hard reset
ARM -> Kb   Reset Ack 1 Reset Ack 1 Hard reset  Hard reset  Hard reset
Kb  -> ARM  Reset Ack 1 Reset Ack 2 Nothing     Nothing     Hard reset
ARM -> Kb   Reset Ack 2 Reset Ack 2 Hard reset  Hard reset  Hard reset
```

The sound system

The sound system is based on the VIDC stereo sound hardware. External analogue anti-alias filters are used which are optimised for a 20 kHz sample rate. The high quality sound output is available from a 3.5mm stereo jack socket at the rear of the machine which will directly drive personal stereo headphones or alternatively an amplifier and speakers. Two internal speakers are fitted, to provide stereo audio.

VIDC sound system hardware

VIDC contains an independent sound channel consisting of the following components: A four-word FIFO buffers 16 8-bit sound samples with a DMA request issued whenever the last byte is consumed from the FIFO. The sample bytes are read out at a constant sample rate programmed into the 8-bit Audio Frequency Register. This may be programmed to allow samples to be output synchronously at any integer value between 3 and 255 microsecond intervals.

The sample data bytes are treated as sine plus 7-bit logarithmic magnitude and, after exponential digital to analogue conversion, de-glitching and sign-bit steering, are output as a current at one of the audio output pins to be integrated and filtered externally.

VIDC also contains a bank of eight stereo image position registers each of three bits. These eight registers are sequenced through at the sample rate with the first register synchronised to the first byte clocked out of the FIFO. Every sample time is divided into eight time slots and the 3-bit image value programmed for each register is used to pulse width modulate the output amplitude between the LEFT and RIGHT audio current outputs in multiples of time slot subdivisions. This allows the signal to be spatially positioned in one of seven stereo image positions.

MEMC sound system hardware

MEMC provides three internal DMA address registers to support Sound buffer output; these control the DMA operations performed following Sound DMA requests from VIDC. The registers allow the physical addresses for the START, PNTR (incremental) and END buffer pointers to a block of data in the lowest half Megabyte of physical RAM to be accessed. These operate as follows: programming a 19-bit address into the PNTR register sets the physical address from which sequential DMA reads will occur (in multiples of four words), and programming the END pointer sets the last physical address of the buffer. Whenever the PNTR register increments up to this END value the address programmed into the START register is automatically written into the PNTR register for the DMA to continue with a new sample buffer in memory. A Sound Buffer Interrupt (SIRQ) signal is generated when the reload operation occurs which is processed by IOC as a maskable interrupt (IRQ) source.

MEMC also includes a sound channel enable/disable signal. Because this enable/disable control signal is not synchronised to the sound sampling, requests will normally be disabled after the waveforms which are being synthesised have been programmed to decay to zero amplitude; the last value loaded into the Audio data latch in the VIDC will be output to each of the Stereo image positions at the current Audio Sample rate.

IOC sound system hardware

IOC provides a programmed output control signal which is used to turn the internal speaker on or off, as well as an interrupt enable/status/reset register interface for the Sound Start Buffer reload signal generated by MEMC.

The internal speakers may be muted by the control line SMUTE which is driven from the IOC output C5. On reset this signal will be taken high and the internal speakers will be muted.

The stereo output to the headphone socket is not muted by SMUTE and will always reflect the current output of the DAC channels.

as well as setting the mouse mode to send data only on RQMP request. SACK enables key scanning and key data transmission but disables unsolicited mouse data. MACK disables key scanning and key data transmission and enables the transmission of mouse count values if either X or Y counts are non-zero. SMAK enables key scanning and both key and mouse data transmission. It combines the enable function of SACK and MACK.

While key scanning is suspended (after NACK or MACK) any new key depression is ignored and will not result in a key down transmission unless the key remains down after scanning resumes following a SACK or SMAK. Similarly, a key release is ignored while scanning is off.

Commands may be received at any time. Therefore, commands can be interleaved with acknowledge replies from the ARM, eg keyboard sends KDDA (first byte), keyboard receives command, keyboard receives BACK, keyboard sends KDDA (second byte), keyboard receives command, keyboard receives SMACK. If the HRST command is received the keyboard immediately enters the restart sequence. The LEDS and PRST commands may be acted on immediately. Commands which require a response are held pending until the current data protocol is complete. Repeated commands only require a single response from the keyboard.

ARM commands

Mnemonic	Function
HRST	Reset keyboard.
LEDS	Turns key cap LEDs on/off. A three bit field indicates which state the LEDs should be in. Logic 1 is ON, logic 0 (zero) OFF. D0 controls CAPS LOCK D1 controls NUM LOCK D2 controls SCROLL LOCK
RQM	Request mouse position (X,Y counts).
RQID	Request keyboard identification code. The computer is manufactured with a 6-bit code to identify the keyboard type to the ARM. Upon receipt of RQID the keyboard controller transmits KBID to the ARM.
PRST	Reserved for future use, the keyboard controller ignores this command.
RQPD	For future use.The keyboard controller will encode the four data bits into the PDAT code data field and then send PDAT to the ARM.

Mouse interface

The mouse interface has three switch sense inputs and two quadrature encoded movement signals for each of the X axis and Y axis directions. Mouse key operations are debounced and then reported to the ARM using the Acorn key up / key down protocol. The mouse keys are allocated unused row and column codes within the main key matrix.

Switch 1 (left)	Row code - 7	Column code - 0
Switch 2 (middle)	Row code - 7	Column code - 1
Switch 3 (right)	Row code - 7	Column code - 2

For example, switch 1 release would give 11010111 (&D7) as th complete row code, followed by 11010000 (&D0) for the column code.

Note: Mouse keys are disabled by NACK and MACK acknowledge codes, and are only enabled by SACK and SMAK codes, ie they behave in the same way as the keyboard keys.

The mouse is powered from the computer 5V supply and may consume up to 100mA.

Movement signals

Each axis of movement is independently encoded in two quadrature signals. The two signals are labelled REFerence and DIRection (eg X REF and X DIR). The table below defines the absolute direction of movement. Circuitry in the keyboard decodes the quadrature signals and maintains a signed 7-bit count for each axis of mouse movement.

Initial state		Next state		
REF	DIR	REF	DIR	
1	1	1	0	
1	0	0	0	Increase count by one
0	0	0	1	for each change of state.
0	1	1	1	
1	1	0	1	
0	1	0	0	Decrease count by one
0	0	1	0	for each change of state.
1	0	1	1	

When count overflow or underflow occurs on either axis both X and Y axis counts lock and ignore further mouse movement until the current data has been sent to the ARM.

Overflow occurs when a counter holds its maximum positive count (0111111 binary). Underflow occurs when a counter holds its maximum negative count (1000000 binary).

the keyboard controller to resend HRST. The pseudo program on the previous page illustrates the reset sequence or protocol.

Note, the on/off state of the LEDs does not change across a reset event, hence the LED state is not defined at power on. The ARM is always responsible for selecting the LED status. After the reset sequence, key scanning will only be enabled if a scan enable acknowledged (SACK or SMAK) was received from the ARM.

Data transmission

When enabled for scanning, the keyboard controller informs the ARM of any new key down or new key up by sending a two byte code incorporating the key row and column addresses. The first byte gives the row and is acknowledged by a byte acknowledge (BACK) code from the ARM. If BACK was not the acknowledge code then the error process (ON error) is entered. If the BACK code was received, the keyboard controller sends the column information and waits for an acknowledge. If either a NACK, SACK, MACK or SMAK acknowledge code is received, the keyboard controller continues by processing the ACK type and selecting the mouse and scan modes implied. If the character received as the second byte acknowledge was not one of NACK/MACK/SACK/SMAK then the error process is entered.

Mouse data

Mouse data is sent by the keyboard controller if requested by a RQMP request from the ARM or if a SMAK or MACK has enabled transmission of non-zero values. Two bytes are used for mouse position data. Byte one encodes the accumulated movement along the X axis while byte two gives Y axis movement.

Both X and Y counts must be transferred to temporary registers when data transmission is triggered, so that accumulation of further mouse movement can occur. The X and Y counters are cleared upon each transfer to the transmit holding registers. Therefore, the count values are relative to the last values sent. The ARM acknowledges the first byte (Xcount) with a BACK code and the second byte (Ycount) with any of NACK/MACK/SACK/SMAK. A protocol failure causes the keyboard controller to enter the error process (ON error).

When transmission of non-zero mouse data is enabled, the keyboard controller gives key data transmission priority over mouse data except when the mouse counter over/underflows.

Acknowledge codes

There are seven acknowledge codes which may be sent by the ARM. RAK1 and RAK2 are used during the reset sequence. BACK is the acknowledge to the first byte of a 2-byte keyboard data set. The four remaining types, NACK/MACK/SACK and SMAK, acknowledge the final byte of a data set. NACK disables key scanning and therefore key up/down data transmission

Code values

Mnemonic	msb	lsb	Comments
HRST	1111	1111	1-byte command, keyboard reset.
RAK1	1111	1110	1-byte response in reset protocol.
RAK2	1111	1101	1-byte response in reset protocol.
RQPD	0100	xxxx	1-byte from ARM, encodes four bits of data.
PDAT	1110	xxxx	1-byte from keyboard, echoes four data bits of RQPD.
RQID	0010	0000	1-byte ARM request for keyboard ID.
KBID	10xx	xxxx	1-byte from keyboard encoding keyboard ID.
KDDA	1100	xxxx	New key down data. Encoded Row (first byte) and column (second byte) numbers.
KUDA	1101	xxxx	Encoded Row (first byte) and column (second byte) numbers for a new key up.
RQMP	0010	0010	1-byte ARM request for mouse data.
MDAT	0xxx	xxxx	Encoded mouse count, X (byte1) then Y (byte2). Only from ARM to keyboard.
BACK	0011	1111	Ack for first keyboard data byte pair.
NACK	0011	0000	Last data byte Ack, selects scan/mouse mode.
SACK	0011	0001	Last data byte Ack.
MACK	0011	0010	Last data byte Ack.
SMAK	0011	0011	Last data byte Ack.
LEDS	0000	0xxx	bit flag to turn LED(s) on/off.
PRST	0010	0001	From ARM, 1-byte command, does nothing.

x is a data bit in the Code; e.g. xxxx is a four bit data field

Key Size	Key Name	Row code	Col. code	Notes
2.25	shift	4	C	1,3
1	Z	4	E	
1	X	4	F	
1	C	5	0	
1	V	5	1	
1	B	5	2	
1	N	5	3	
1	M	5	4	
1	,<	5	5	
1	.>	5	6	
1	/	5	7	
2.75	shift	5	8	1,3
1	crsrUp	5	9	1
1	1	5	A	
1	2	5	B	
1	3	5	C	
1.5	Caps	5	D	1,4
1.5	Alt	5	E	1,3
7.0	Space	5	F	
1.5	Alt	6	0	1,3
1.5	Ctrl	6	1	1,3
1	crsrLt	6	2	1
1	crsrDn	6	3	1
1	crsrRt	6	4	1
2.0	0	6	5	
1	.	6	6	
2.0	Enter	6	7	1

Row and column codes are in hexadecimal.

Notes:
1 Key colour - dark grey.
2 Key colour - red.
3 Key position with N key rollover.
4 Green LED under key cap.

Keyswitch mapping

Key size	Key name	Row code	Col. code	Notes
1	Esc	0	0	1
1	F1	0	1	2
1	F2	0	2	2
1	F3	0	3	2
1	F4	0	4	2
1	F5	0	5	2
1	F6	0	6	2
1	F7	0	7	2
1	F8	0	8	2
1	F9	0	9	2
1	F10	0	A	2
1	F11	0	B	2
1	F12	0	C	2
1	Print	0	D	1,3
1	Scroll	0	E	1
1	Break	0	F	1
1	~	1	0	
1	1	1	1	
1	2	1	2	
1	3	1	3	
1	4	1	4	
1	5	1	5	
1	6	1	6	
1	7	1	7	
1	8	1	8	
1	9	1	9	
1	0	1	A	
1	-_	1	B	
1	=+	1	C	
1	£¤	1	D	
1	Backspc	1	E	1
1	Insert	1	F	1
1	Home	2	0	1,3
1	Pgup	2	1	1
1	Numlock	2	2	1,4
1	/	2	3	1
1	*	2	4	1
1	#	2	5	1

Key size	Key name	Row code	Col. code	Notes
1.5	Tab	2	6	1
1	Q	2	7	
1	W	2	8	
1	E	2	9	
1	R	2	A	
1	T	2	B	
1	Y	2	C	
1	U	2	D	
1	I	2	E	
1	O	2	F	
1	P	3	0	
1	[{	3	1	
1	]}	3	2	
1.5	\	3	3	
1	Delete	3	4	1
1	Copy	3	5	1
1	Pgdwn	3	6	1
1	7	3	7	
1	8	3	8	
1	9	3	9	
1	-	3	A	1
1.75	Ctrl	3	B	1,3
1	A	3	C	
1	S	3	D	
1	D	3	E	
1	F	3	F	
1	G	4	0	
1	H	4	1	
1	J	4	2	
1	K	4	3	
1	L	4	4	
1	;:	4	5	
1	,"	4	6	
2.25	Return	4	7	1
1	4	4	8	
1	5	4	9	
1	6	4	A	
1	+	4	B	1

Row and column codes are in hexadecimal.

Notes:
1. Key colour - dark grey.
2. Key colour - red.
3. Key position with N key rollover.
4. Green LED under key cap.

Links

Link	Fitted	Effect	Default
LK22	Yes	Connection point for left channel audio speaker. P1 0V, P2 signal.	None
LK23	Yes	Connection point for right channel audio speaker. P1 0V, P2 signal.	None
LK5	No	Connection point for an external battery. (Only used if supply of on board NiCad becomes a problem.)	None
LK20	Yes	Used in conjunction with LK19 to select size of ROM devices.	Shunt 2-3
LK19	Yes	Used in conjunction with LK20 to select size of ROM devices. ROM LK19 LK20 512K 2-3 2-3 1M 2-3 2-3 2M 1-2 2-3 4M 1-2 1-2	Shunt 2-3 ie 1M
LK25	Yes	Used to configure P5 of SK14 (RGB Video Socket) to be either 'VSync' or 'Mode'. Fit shunt for 'VSync' NF shunt for 'Mode' (Mode is required by some SCART TVs.)	Shunt NF ie 'Mode'
LK24	Yes	Used to configure P4 of SK14 (RGB Video Socket) to be either 'HSync' or 'CSync'. Shunt , 1-2 for 'HSync' Shunt , 2-3 for 'CSync'	Shunt 2-3 ie 'CSync'
LK27	Yes	Used to invert 'VSync'. Shunt fitted , VSync* Shunt NF, VSync	Shunt NF ie 'VSync'
LK26	Yes	Used to invert 'HSync'. Shunt fitted , HSync* Shunt NF, HSync	Shunt NF ie 'HSync'
LK7	No	Test point for Non Volatile Memory clock frequency. P1 0V P2 32.768KHz	None
LK30	No†	Used in conjunction with LK29 and LK28 (& 31 on Iss1) to provide the necessary signals for a Genlock interface circuit. P1 VS* P2 HS*	None
LK28	No†	P1 Ckvidc P2 Clksys*	Trk 1-2 (Shunt on Iss1)
LK29	No†	P1 0V P2 Sink	Trk 1-2 (Shunt on Iss1)
LK31	No†	P1 'Sup' P2 0V	None
LK6	No	Test point for Non Volatile Memory battery voltage. P1 0V P2 1.2V +- 0.2V	None

Link	Fitted	Effect	Default
LK8 LK9 LK10 LK11 LK12 LK13	No No No No No No	Used to set nationality id of the keyboard.	LK12 Trk ie UK
LK1 LK2	No No	Used to optionally link 0V to the RFI Shield (Earth).	NF NF
LK3	No	Connection point for a design backup, self contained keyboard. P1 Krst * Keyboard Reset P2 NC P3 0V P4 5V P5 Krx* From keyboard P6 Ktx* To keyboard	NF
LK4	No	Connection point for design backup, mouse to keyboard link. P1 Xr X ref P5 Sw(1) Switch 1 P2 Xd X dir P6 Sw(2) Switch 2 P3 Yr Yref P7 Sw(3) Switch 3 P4 Yd Ydir P8 0V	NF
LK17	No†	Used in conjunction with LK18 to select ROM device type.	Trk 1-2 (Shunt on Iss1)
LK18	No†	Used in conjunction with LK17 to select ROM device type. ROM LK17 LK18 512K EPROM 1-2 1-2 Non JEDEC 1M ROM 1-2 1-2 Non JEDEC 1M EPROM 1-2 1-2 JEDEC 1/2/4M ROM/ EPROM 1—1, 2—2	Trk 1-2 ie Non JEDEC (Shunt on Iss1)
LK16	No	Used to select the design backup keyboard. See LK3. 1-2 Selects backup keyboard 2-3 Selects main keyboard	Trk 2-3 ie Main K/B
LK21	No	Selects the +5V power feed to the floppy disc drive to be via the data cable or by separate feed. 1-2 +5V via data cable 2-3 +5V via separate cable	Trk 2-3 ie not via data cable
LK14 LK15	No No	Used in conjunction with LK15 to select the keyboard uC device type. Device Type LK14 LK15 8051 (NMOS) 1-2 1-2 80C51 (CMOS) O/C 2-3	Trk 1-2 Trk 1-2 ie NMOS
LK32	No	Provides access to RGB interface signals (Issue 1 only): 1 - Red 4 - H/CSYNCH 2 - Green 5 - VSYNC/MODE 3 - Blue 6 - 0V	NF

Notes:
NF - Not Fitted
P1 - Pin 1
O/C - Open Circuit
Trk - Tracked
* Active low
† Fitted on Issue1 PCB

Floppy disc drive

The floppy disc drive used on the A3000 computer is a one-inch high drive, taking 3.5 inch floppy discs.

Performance

Capacity	1 MB (unformatted)
Track to track step rate	3ms
Seek settle time	15ms
Write to read timing	1200µs
Power-on to drive ready	1000ms
Power supply	+5Vdc (+/– 5%)
Noise bandwidth	0 – 30 MHz
Maximum power	2 Watts (continuous)

Power connector

The power connector is a 4-pin, 25mm pitch type. The LED is ON when Drive Select and In Use are low or when Drive Select is low.

Pin	Signal
1	+5
2	Ground
3	Ground
4	No connection

Interface connector

The interface connector is a 34-way, 2 row, 0.1 inch pitch type, with pinouts as shown below:

Pin		Signal	Dir
Retn	Signal		(pcb)
1	2	Disc change	I
3	4	In use	I
5*	6	Drive select 3	O
7*	8	Index	I
9*	10	Drive select 0	O
11*	12	Drive select 1	O
13	14	Drive select 2	O
15	16	Motor ON	O
17	18	Direction	O
19	20	Step/Dsc chg rst	O
21	22	Write data	O
23	24	Write gate	O
25	26	Track 0	I
27	28	Write protect	I
29	30	Read data	I
31	32	Side 1 select	O
33	34	Ready	I

*Optionally 5V

Power supply

Performance characteristics

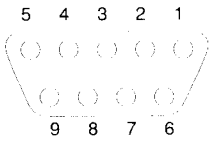
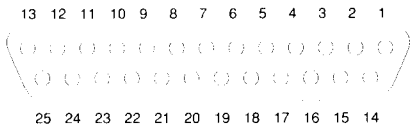
Performance	Min	Nom	Max	Units
Input voltage (47-53 Hz)	198	220/ 240	264	Vac
Input voltage (57-63 Hz)	99	115	130	Vac
Output voltage VO1	4.9	5	5.1	Vdc
Output current IO1	0.5		4.4	Amps dc
Ouput ripple and noise VO1				50mV pk-pk BW 0-50MHz
Overshoot VO1				0.1Vdc
Overvoltage prot VO1 (thrshld)	5.8	-	7.0	Vdc
Surge output current IO1	-	-	5.8	Amps dc
Surge output current duration	-	-	1.0	Sec
Efficiency	65	-	-	%@max Id
Total output power	-	-	22	Watts cont 29 Watts srge

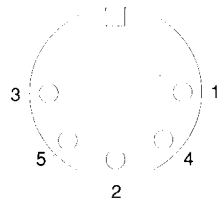
Input voltage is selected by means of a link wire connected either to the pin marked '240' on the lefthand side of the power supply (when facing the front of the computer), or to the pin marked '120' in the top centre of the PSU. If the input voltage is changed, it is strongly recommended that a label, indicating the new voltage to which the computer has been set, is fixed to the outside of the case. A mains plug appropriate to the new supply should also be fitted, to prevent the computer from being powered up at the wrong voltage.

Floppy disc power connector

Pin	Signal
1	+5V
2	0V
3	N C
4	N C

Sockets (contd)

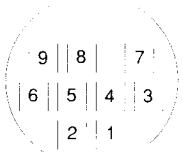
No.	Fitted	Function/Specification
SK14	Yes	RGB Video Socket. 9-way D-type socket providing an interface to analogue RGB monitors and Scart TVs. Links 24, 25, 26 & 27 can be used to alter the polarity and type of syncronisation signals present to suit a variety of monitors. RGB Video levels , 0.7V Pk-Pk into 75 Ohm Sync Voltage levels , >= 2.0V (TTL)  Pin Signal (IBM PC PGA pinning) 1 Red 2 Green 3 Blue 4 H/Csync 5 Vsync/Mode 6,7,8,9 0V
SK13	Yes	Monochrome Video Output. Phono socket providing a monochrome composite video signal of 1V Pk-Pk (0.7V video, 0.3V Sync) into a 75 Ohm load. Negative sync, positive video.
SK12	Yes	Stereo Headphone Output. 3-way 3.5mm stereo jack socket providing output to personal stereo type 32 Ohm stereo headphones. Output voltage = 1V Pk-Pk into 32 Ohm load.
SK15	Yes	External Podule Expansion. 64 Way DIN41612 socket providing an interface connection to a single, host powered, external Podule. This Podule may be a 'MEMC' or 'Simple' type but not a Co-processor. For a full spec of this interface see the chapter entitled 'A3000 expansion'.
SK10	Yes	Parallel Printer Port. 25-way D-type socket providing a parallel printer interface.  Pin Signal Pin Signal Pin Signal 1 Stb* 8 Pd(6) 15 nc 2 Pd(0) 9 Pd(7) 16 nc 3 Pd(1) 10 Ack* 17/25 0V 4 Pd(2) 11 Bsy 5 Pd(3) 12 nc 6 Pd(4) 13 nc 7 Pd(5) 14 nc

No.	Fitted	Function/Specification
SK2	Yes	Econet Socket. 5-way Din socket for connection to Econet local area network. Note, this interface is an upgrade.  Pin Signal 1 Data 2 0V 3 Clock* 4 Data* 5 Clock
SK5	Yes	Econet Upgrade Module Socket. 5 way header used in conjunction with SK4 to provide electrical connections for the Econet upgrade module. This module is identical to that used on BBC Master series and Archimedes microcomputers.

Plugs

Plug	Fitted	Function/Specification
PL5	No	Floppy Disc Power Connector. If the power to the disc drive is to be supplied via the data cable, then PL5 must be fitted and the PSU free disc power socket must be connected to this plug. P1 NC P2 0V P3 0V P4 +5V
PL6	No	Floppy Disc Drive Data Connector. 34-way Box Header containing all the signals required by the internal floppy disc drive. This interface is identical to that of the Archimedes, except that the drive strength of some of the signals has been reduced as only one drive is supported. The pin numbering has been altered due to the incorrect orientation of the Archimedes layout. Default powering is via a separate power connector from the PSU (ie not up the data cable). Pin Signal Pin Signal 2 Dcirq* 20 Step* 4 Inuse* 22 Writedata* 6 Sel(3)* 24 Writegate* 8 Index* 26 Track00* 10 Sel(0)* 28 Writeprot* 12 Sel(1)* 30 Readdata* 14 Sel(2)* 32 Side1* 16 Motoron* 34 Ready* 18 Dirin* 1,3,5,7,9,11,13,15,17,19,21,23,25,27,29,31,33 all 0V
PL1	Yes	Faston tab for connection of earth from the power supply.
PL3	Yes	Faston tab for connection of 0V from the power supply.
PL4	Yes	Faston tab for connection of +5V from the power supply.
PL2	Yes	Serial Port. (IBM PC-AT Pinout) 9-way D-type plug. Although the plug is fitted, the interface electronics are an upgrade consisting of: IC 7 LT1133 IC 1 65C51 Pin Signal Pin Signal 1 Dcd 6 Dsr 2 Rxd 7 Rts 3 Txd 8 Cts 4 Dtr 9 Ri 5 0V

Sockets

No.	Fitted	Function/Specification
SK1	Yes	Mouse Port. 9-way MiniDin socket providing interface to a standard Acorn (Archimedes style) mouse.  Pin Signal 1 Xr X direction reference 2 Sw(1) Switch 1 3 Sw(2) Switch 2 4 0V 0V 5 Xd X direction 6 +5V +5V 7 Yr Y direction reference 8 Sw(3) Switch 3 9 Yd Y direction
SK4	Yes	Econet Upgrade Module Socket. 17-way header used in conjunction with SK5 to provide the electrical connection point for the internal Econet upgrade module. This module is identical to that used in the BBC Master series and Archimedes computers.
SK16	Yes	Ram Upgrade Connector. A 60-way SIL pin row, providing all the necessary signals for the Acorn 1MByte Ram upgrade card.
SK3 SK11 SK8 SK9	Yes Yes No† No†	Internal Expansion. These connectors jointly form the internal expansion facility and are in the form of two17-way headers for SK3 & 11 and two 5-way headers for SK8 & 9. SK3 & SK11 form an 8-bit 'simple' podule bus SK3, 11, 8 & 9 form an 8-bit MEMC podule bus. A full specification of this expansion interface is provided in the chapter headed 'A3000 Expansion'.
SK6 SK7	Yes Yes	Keyboard Interface. Two 20-way 'flexible PCB' connectors providing an interface to the keyboard.

Notes:

† Fitted to Issue 1 PCBs

Socket diagrams are viewed from outside the computer

RGB & SYNC

A 6-way connector (LK32, not fitted) has been added to RGB & SYNC for internal access.

Production changes

The components R550, C55, C78, C500, C501 and C504 have been moved to facilitate production.

R145 (4K7 SMD 5%) has been added between IC2 pin 31 and +5V to accomodate ATE.

Test points have been added to the following lines:
ARM20-MEMC3
MEMC38
MEMC39
MEMC40
MEMC41
MEMC42
(R129-R132 have been moved to accomodate these test points.) .

Changes between Issue A and Issue 1 PCBs

This manual covers A3000s produced with both Issue A and Issue 1 PCBs, and drawings for both versions are included. This section summarises the changes made during the production of Issue A boards, and the design changes made for Issue 1..

Modifications to Issue A PCBs

Component value changes

The chart below summarises the component value changes made during the production of Issue A PCBs, showing the first serial number changed.

(Unless otherwise stated, resistors are 5% SMD.)

Comp.	Issue A	Changed to	Serial no.
R67	68R	22R	1000051
R68	68R	22R	1000051
R69	68R	22R	1000051
R70	68R	22R	1000051
R71	68R	22R	1000051
R81	33K	3K3	1000013
R82	150K 1%	22K 1%	1000013
R85	33K	3K3	1000013
R86	150K 1%	22K 1%	1000013
R88	33K	3K3	1000013
R89	33K	3K3	1000013
R91	150K 1%	22K 1%	1000013
R92	33K	3K3	1000013
R93	150K 1%	22K 1%	1000013
R95	150K 1%	22K 1%	1000013
R97	150K 1%	22K 1%	1000013
R98	150K 1%	22K 1%	1000013
R99	150K 1%	22K 1%	1000013
R101	33K	3K3	1000013
R105	470R	680R	1000051
R129	33R	22R	1000051
R130	33R	22R	1000051
R131	33R	22R	1000051
R132	33R	22R	1000051
R133	33R	22R	1000051
R137	100K	10K	1000051
R502	6K8	4K7	1000013
R530	22K	1K	1004150
C75	100p CPLT	2n2 CPLT 10%	1000013
C77	2n7 CPLT	22n MPSTR 10%	1000013
C80	22n MPSTR	100n MPSTR 10%	1000013
C81	330p	2n2 CPLT	1000013
C82	330p	2n2 CPLT	1000013
C86	330p	2n2 CPLT	1000013
C88	22n MPSTR	100n MPSTR 10%	1000013
C90	100p CPLT	2n2 CPLT 10%	1000013
C91	330p	2n2 CPLT	1000013
C92	2n7 CPLT	22n MPSTR 10%	1000013

The following additional modifications were made during the production of Issue A PCBs:

Serial interface

10K resistor (5%, conventional type) was added as a 'pullup' to the rear of the PCB, connected between the signal Rii* (IC7 pin 18) and +5V (from serial number 1000001).

Video genlocking

The tracks on the underside of the PCB, between the pins of both LK28 and LK29, were cut. 2-pin wafers were fitted to LK28, 29 & 30, and shunts to LK28 and 29 (but not LK30) (from 1000251).

I^2C-bus access

Two 5-way headers (0800,486) were fitted to SK8 and SK9 (from 1000251).

JEDEC & non-JEDEC EPROMs

To permit the use of JEDEC and non-JEDEC EPROMs, tracks on the PCB, between the pins of both LK17 and LK18, were cut. 2-pin wafers were fitted to LK17 and LK18, and shunts fitted to LK17 and 18 (from 1000251).

Fixing of 64W connector

Two rivets (Avdel 11070312) were added to the mounting holes of the 64-way expansion connector.

Design changes made between Issue A and Issue 1PCBs

Serial interface

The 'strapped on' resistor (see above) was replaced by a permanent resistor (10K SMD 5%) – R144.

Signal conditioning

R141, R142 and R143 have been added (22R SMD 5%) to REF8M, RA9 and IORQ. R134 has been moved to accomodate these.

A capacitor C116 (2n7) has been added between SW3 and 0V.

Video genlocking

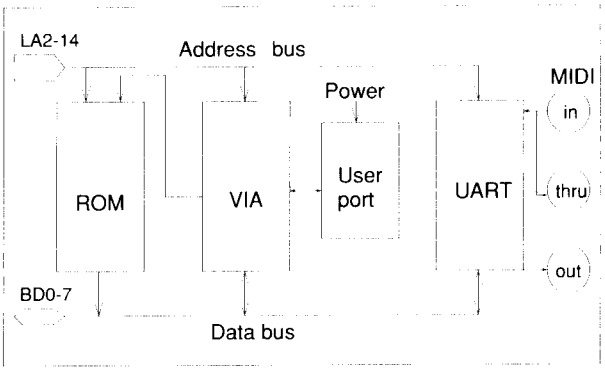
LK28 & 29 tracks have been deleted (see above). LK28, 29 & 30 moved.

LK31 has been added. This allows access to the VIDC supremacy bit (pin 28) and GND.

JEDEC & non-JEDEC EPROMs

The tracks between the pins of LK17 & 18 have been deleted (see above).

Block diagram



Comparison with Archimedes expansion cards

ARCHIMEDES I/O EXPANSION CARD

- The VIA is at the same address and clocked at the same speed. Port A PA<0..2> is used to page ROM. These are the same as the UPM when set for 2764/27128.
- The User port is the same (Port B). The VIA interrupts go through a link, which is not normally fitted.
- The MIDI section is not the same.
- The ADC and 1 MHz bus are not fitted to the UPM.

MIDI EXPANSION CARD

- The UART is the same (Signetics 2691), but is at a different address (see below).
- The ROM page latch is not the same.

	LA13	LA12	offset address
MIDI Podule	1	0	&2000
UPM upgrade	1	1	&3000

Addresses of main system components

Address	Component
&0000-1FFC	ROM/EPROM 27128 as standard (16k x 8 bit). Larger EPROMS can be fitted if the links marked X are cut between pins 1 & 2, and relinked 2 to 3.

Eprom size	LK1	LK2	LK3	LK4
2764				
27128				
27256			X	
27512	X		X	
1M bit (JEDEC)	X		X	
2M bit	X	X	X	
4M bit	X	X	X	X

	Contains the ID byte 63 (dec).
	The startup information must be at the top of the ROM.
&2000-2FFC	VIA 65C22 - 2Mhz part.
	Port A PA<7..0> used to page the ROM. CAs Not Used.
	Port B PB<7..0>, CB1 and CB2 for the User Port.
	Use 2Mhz synchronous cycle to access the VIA.
	The interrupt output connects directly to PIRQ*.
	No User Port interrupt handler provided.
&3000-3FFC	UART 2691 - For the MIDI interface.

A3000 Expansion

Internal expansion

> DANGER
>
> DANGEROUS VOLTAGES MAY BE EXPOSED INSIDE THE CASE OF THE COMPUTER WHEN THE COVER IS REMOVED. THE COMPUTER SHOULD BE DISCONNECTED FROM THE MAINS SUPPLY BEFORE THE COVER IS REMOVED.

The following internal upgrades are currently available from Acorn for the A3000 computer:

- User port/MIDI internal expansion card
- 1 Mb Ram upgrade
- Serial port
- Econet module.

Internal upgrades must be fitted by an Acorn Dealer or Approved Service Centre. Instructions on how to fit the upgrades are given in the A3000 Service Manual.

Interface

The electrical signals available on the internal expansion are a subset of those described in 'A Series podules', available from Acorn Customer Service as an Application Note, or on the SID system (Document Reference 0310101).

The connection is via two 17-way 0.1 inch pitch connectors and two 5-way 0.1 inch connectors (the latter fitted as standard to Issue 1 PCBs and later). Expansion cards should use 0.025 inch square pin headers.

Expansion bus connectors

Pin no	SK3	SK11*	SK8	SK9
1	+5V	0V	C[0]	0v
2	PWE*	+5V	C[1]	REF8M
3	PS1*	PRE*	BI*	PFIQ*
4	CLK2	PR/nW	IORQ*	Ms[1]*
5	LA[2]	LA[4]	IOGT*	+5V
6	LA[3]	LA[5]		
7	BD[0]	LA[6]		
8	BD[1]	LA[7]		
9	BD[2]	0V		
10	BD[3]	LA[8]		
11	BD[4]	LA[9]		
12	BD[5]	LA[10]		
13	BD[6]	LA[11]		
14	BD[7]	LA[12]		
15	RST*	LA[13]		
16	0V	PIRQ*		
17	+5V	0V		

Note: Pin 1 is at the righthand end when viewed from the front of the computer.

The interface is configured as 'Podule 1, Module 1'.

It is recommended that the load on each signal does not exceed 3HCT gates or that stated in 'A Series podules'. Any upgrade must be able to drive at least 7 HCT and 3 TTL loads on the data bus.

Power supply

The maximum power available from the +5V rail is 600 mA. The maximum dissipation inside the case is 0.5W (100mA).

Mechanical

The rear panel required is shown in the drawing at the back of this manual. The size of the User Port/MIDI expansion card PCB and position of the connectors are also shown in the drawing at the back of the manual.

User Port/MIDI expansion card (UPM)

Introduction

The A3000 User Port / MIDI expansion card fits inside the computer, and provides:

- An 8-bit User Port, largely compatible with the User Port interface on the BBC Model B and Master 128 microcomputers (and with the User Port on the Archimedes I/O expansion card).
- MIDI (Musical Instrument Digital Interface), with IN, OUT and THRU connections, compatible with the International MIDI Association specification.

Main components

- 65C22 VIA for the User Port
- 2691 UART for the MIDI
- 27128 EPROM containing firmware and ID byte.

External expansion connections

Pin	a	c	Description
1	0V	0V	Ground
2	LA[15]	reserved	
3	LA[14]	0V	Ground
4	LA[13]	0V	Ground
5	LA[12]	reserved	
6	LA[11]	MS[0]*	MEMC Podule select
7	LA[10]	reserved	
8	LA[9]	reserved	
9	LA[8]	reserved	
10	LA[7]	reserved	
11	LA[6]	reserved	
12	LA[5]	RST*	Reset (see note below)
13	LA[4]	PR/W	Read/not write
14	LA[3]	PWE*	Write strobe
15	LA[2]	PRE	Read strobe
16	BD[15]	PIRQ*	Normal interrupt
17	BD[14]	PFIQ	Fast interrupt
18	BD[13]	S[6]*	
19	BD[12]	C1	I²C serial bus clock
20	BD[11]	C0	I²C serial bus data
21	BD[10]	S[7]*	External Podule select
22	BD[9]	PS[0]	Simple Podule select
23	BD[8]	IOGT*	MEMC Podule handshake
24	BD[7]	IORQ	MEMC Podule request
25	BD[6]	BL*	I/O data latch control
26	BD[5]	0V	Supply
27	BD[4]	CLK2	2MHz Synchronous clock
28	BD[3]	CLK8	8MHz Synchronous clock
29	BD[2]	REF8M	8MHz Reference clock
30	BD[1]	+5V	Supply
31	BD[0]	reserved	
32	+5V	reserved	

Note: The RST* signal is the system reset signal, driven by IOC on power up or by the keyboard reset switch. It is an open-collector signal, and expansion cards *may* drive it also if this is desirable. The pulse width should be at least 50ms.

2Mb RAM upgrade

The A3000 computer RAM can be upgraded from 1Mb to 2Mb by the addition of a 1Mb RAM module which plugs into the main PCB.

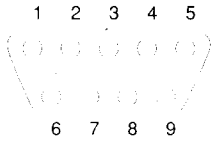
Serial port upgrade

Introduction

The A3000 computer is fitted with a 9-way D-type serial connector on the back panel, but this is not functional until a serial port upgrade kit has been fitted by an Acorn Dealer or Approved Service Centre. Only Acorn Serial Port Upgrade kits should be used.

The A3000 serial port upgrade consists of a serial processor chip (C 65C51) and a line driver chip (LT1133), which fit into existing sockets on the PCB. The C 65C51 fits into socket IC1, and the LT1133 into socket IC7.

Connector pinouts



Pin	Signal	Pin	Signal
1	DCD	6	OSR
2	RXD	7	RTS
3	TXD	8	CTS
4	DTR	9	RI
5	0V		

External expansion

Interface

Introduction

The A3000 computer supports an external expansion card (podule) interface, although with some minor differences from other ARM based systems:

- Single +5V power supply rail, rated at a maximum of 1 Amp (no +12 or -5V rails provided)
- No support for Co-Processor type cards
- The external expansion card is in software slot 0
- The podule must be capable of driving 3 TTL and 7HCT loads on the data bus.

Refer to the application note 'A Series podules' (referenced at the start of this chapter) for a full podule interface specification.

Physical dimensions

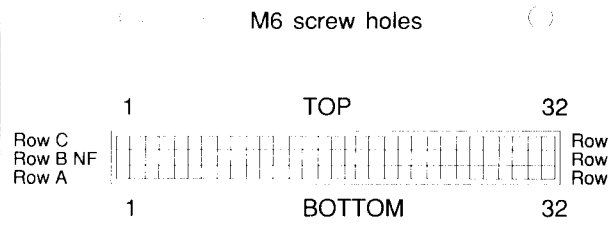
As the podule is external to the computer enclosure there is no real limit on the size of the unit. Care should be taken not to block off any of the other expansion ports on the rear of the computer.

External expansion units

It is anticipated that expansion cards will be fitted into an external expansion unit. Slots are provided underneath the case of the computer, into which a tongue in the case of the expansion card unit can locate. Tapped holes are provided in the backplate of the computer to enable an expansion unit to be secured to the computer with two M6 screws. The diagram at the back of the manual shows the provisions made on the computer for fitting such an external expansion unit.

Connector

The podule interface is provided via a 64-way DIN 41612 socket fitted at the rear of the computer:



(Connector viewed from the back of the computer)

Item	Description	Qty
R88	RES 3K3 SMD 5% 0W25 1206	1
R89	RES 3K3 SMD 5% 0W25 1206	1
R90	RES 56R SMD 5% 0W25 1206	1
R91	RES 22K MF 1% 0W25	1
R92	RES 3K3 SMD 5% 0W25 1206	1
R93	RES 22K MF 1% 0W25	1
R94	RES 56R SMD 5% 0W25 1206	1
R95	RES 22K MF 1% 0W25	1
R96	RES 332R MF 1% 0W25 E96	1
R97	RES 22K MF 1% 0W25	1
R98	RES 22K MF 1% 0W25	1
R99	RES 22K MF 1% 0W25	1
R100	RES 33R SMD 5% 0W25 1206	1
R101	RES 3K3 SMD 5% 0W25 1206	1
R102	RES 43R2 MF 1% 0W25 E96	1
R103	RES 43R2 MF 1% 0W25 E96	1
R104	RES 43R2 MF 1% 0W25 E96	1
R105	RES 680R SMD 5% 0W25 1206	1
R106	RES 10K SMD 5% 0W25 1206	1
R107	RES 10K SMD 5% 0W25 1206	1
R108	RES 330R SMD 5% 0W25 1206	1
R109	RES 10K SMD 5% 0W25 1206	1
R110-R115	RES 1K00 MF 1% 0W25 E96	4
R114	RES 1K2 SMD 5% 0W25 1206	1
R115-R128	RES 68R SMD 5% 0W25 1206	14
R129-R133	RES 22R SMD 5% 0W25 1206	5
R134	RES 1K2 SMD 5% 0W25 1206	1
R135	RES 33R SMD 5% 0W25 1206	1
R136	RES 220R SMD 5% 0W25 1206	1
R137	RES 10K SMD 5% 0W25 1206	1
R138	RES 68R SMD 5% 0W25 1206	1
R139	RES 68R SMD 5% 0W25 1206	1
R140	RES 68R SMD 5% 0W25 1206	1
R141	RES 22R SMD 5% 0W25 1206	1
R142	RES 22R SMD 5% 0W25 1206	1
R143	RES 22R SMD 5% 0W25 1206	1
R144	RES 10K SMD 5% 0W25 1206	1
R145	RES 4K7 SMD 5% 0W25 1206	1
R500	RES 33K SMD 5% 0W25 1206	1
R50	RES 10K SMD 5% 0W25 1206	1
R502	RES 4K7 SMD 5% 0W25 1206	1
R503-R518	RES 68R SMD 5% 0W25 1206	16
R519-R529	RES 100K SMD 5% 0W25 1206	11
R530	RES 1K0 SMD 5% 0W25 1206	1
R531	RES 180R SMD 5% 0W25 1206	1
R532	RES 82R SMD 5% 0W25 1206	1
R533	RES 330R SMD 5% 0W25 1206	1
R534	RES 68R SMD 5% 0W25 1206	1
R535	RES 68R SMD 5% 0W25 1206	1
R536	RES 220R SMD 5% 0W25 1206	1
R537	RES 68R SMD 5% 0W25 1206	1
R538	RES 220R SMD 5% 0W25 1206	1
R539	RES 68R SMD 5% 0W25 1206	1
R540	RES 220R SMD 5% 0W25 1206	1
R541	RES 68R SMD 5% 0W25 1206	1
R542	RES 220R SMD 5% 0W25 1206	1
R543-R5	RES 1K0 SMD 5% 0W25 1206	4
R547	RES 4K7 SMD 5% 0W25 1206	1
R548	RES 4K7 SMD 5% 0W25 1206	1
R549	RES 100K SMD 5% 0W25 1206	1
R550	RES 4K7 SMD 5% 0W25 1206	1
R551	RES 4K7 SMD 5% 0W25 1206	1
R552	RES 4K7 SMD 5% 0W25 1206	1
R553	RES 220R SMD 5% 0W25 1206	1
R554	RES 10K SMD 5% 0W25 1206	1
R555		N/F
R556		N/F
R557	RES 47K SMD 5% 0W25 1206	1
R558		N/F
R559		N/F
R560	RES 330R SMD 5% 0W25 1206	1
R561	RES 270R SMD 5% 0W25 1206	1
R562		N/F
R563		N/F
R564	RES 47K SMD 5% 0W25 1206	
R565	RES 47K SMD 5% 0W25 1206	1
R566		N/F
R567-R571	RES 47K SMD 5% 0W25 1206	5
R572	RES 220R SMD 5% 0W25 1206	1
R573-R579		N/F
C1	PCPCTR DCPLR 33n SMD 1210	1
C2	CPCTR CPLT 33p 30V 2%	1
C3	CPCTR CER 47n 30V 80%	1
C4	CPCTR TANT 10u 10V 20%	1
C5	CPCTR DCPLR 33n SMD 1210	1
C6-C10	CPCTR ALEC 10u 16V RAD	5
C11	CPCTR DCPLR 33n SMD 1210	1
C12	CPCTR ALEC 220u 16V RAD	1
C13	CPCTR TANT 10u 10V 20%	1
C14	CPCTR ALEC 220u 16V RAD	1
C15	CPCTR ALEC 47u 16V RAD	1
C16	CPCTR CPLT 12p 30V 2%	1
C17	CPCTR DCPLR 33n SMD 1210	1
C18	CPCTR DCPLR 33n SMD 1210	1
C19	CPCTR ALEC 10u 16V RAD	1
C20	CPCTR DCPLR 33n SMD 1210	1
C21	CPCTR DCPLR 33n SMD 1210	1
C22	CPCTR TANT 10u 10V 20%	1
C23	CPCTR CPLT 100p 30V 2%	1
C24-C31	CPCTR CPLT 2n2 30V 10%	8
C32	CPCTR CPLT 100p 30V 2%	1
C33	CPCTR CPLT 100p 30V 2%	1
C34	CPCTR TANT 10u 10V 20%	1
C35	CPCTR DCPLR 33n SMD 1210	1
C36	CPCTR DCPLR 33n SMD 1210	1
C37	CPCTR DCPLR 33n SMD 1210	1
C38		N/F
C39	CPCTR ALEC 47u 10V AX	1
C40-C47	CPCTR DCPLR 33n SMD 1210	8
C48	CPCTR DCPLR 100n SMD 1210	1
C49	CPCTR DCPLR 100n SMD 1210	1
C50-C54	CPCTR DCPLR 33n SMD 1210	5
C55	CPCTR TANT 10u 10V 20%	1
C56	CPCTR DCPLR 100n SMD 1210	1
C57	CPCTR TANT 10u 10V 20%	1
C58	CPCTR DCPLR 100n SMD 1210	1
C59	CPCTR DCPLR 33n SMD 1210	1
C60	CPCTR ALEC 47u 16V RAD	1
C61	CPCTR ALEC 220u 16V RAD	1
C62	CPCTR CER 47n 30V 80%	1
C63	CPCTR ALEC 47u 16V RAD	1
C64	CPCTR DCPLR 33n SMD 1210	1
C65	CPCTR ALEC 100u 25V RAD	1
C66	CPCTR ALEC 220u 16V RAD	1
C67	CPCTR ALEC 4u7 16V RAD	1
C68	CPCTR CER 47n 30V 80%	1
C69	CPCTR ALEC 220u 16V RAD	1
C70	CPCTR ALEC 100u 25V RAD	1
C71	CPCTR DCPLR 100n SMD 1210	1
C72	CPCTR DCPLR 100n SMD 1210	1
C73	CPCTR DCPLR 100n SMD 1210	1
C74	CPCTR CER 47n 30V 80%	1
C75	CPCTR CPLT 2n2 30V 10%	1
C76	CPCTR DCPLR 33n SMD 1210	1
C77	CPCTR MPSTR 22n 50V 10%	1
C78	CPCTR TANT 10u 10V 20%	1
C79	CPCTR CPLT 1n 30V 10%	1
C80	CPCTR MPSTR 100n 50V 10%	1
C81	CPCTR CPLT 2n2 30V 10%	1
C82	CPCTR CPLT 2n2 30V 10%	1
C83	CPCTR ALEC 47u 10V AX	1
C84	CPCTR DCPLR 100n SMD 1210	1

Parts lists

The parts lists in this chapter detail the components used in the manufacture of the computer and its upgrades. Contact the Spares Department of Acorn Computers Limited (account holders only), or its authorised dealers and Approved Service Centres, for information as to which parts are available as spares.

Final assembly parts list

Item	Description	Qty
1	FINAL ASSEMBLY DRAWING	1*
3	DISC DRIVE CABLE ASSY	1
4	'NO ECONET' LABEL	1
5	RESET BUTTON	1
7	A3000 MAIN PCB ASSY	1
8	22W 240V PSU	1
9	KEYBOARD {UK}	1
10	MAINS CABLE ASSY	1
11	SPEAKER ASSEMBLY	2
12	3.5x1" 1MB DISC DRIVE	1
14	LOWER MOULDING	1
15	UPPER MOULDING	1
16	BATTERY COVER	1
17	BLANKING PANEL	1
18	LOCK PLATE	2
19	CABLE RESTRAINT PLATE	1
20	PSU COVER	1
21	PSU INSULATION SHEET	1
23	BBC/LED LABEL	1
24	BASE LABEL	1
25	'NO SERIAL' LABEL	1
26	REAR MAINS LABEL	1
27	ACORN LOGO LABEL	1
29	GRMT CBL RND 7.4Dx4T BLK	1
30	ADH HOT-MELT	A/R
31	SCW No2x1/4" PLST PAN POS	1
32	SCW No4x1/4" PLST PAN POS	2
33	SCW M2.5x6 PAN HD POSI	4
34	SCW M3x6 PAN HD POSI	4
35	SCW No4x3/4" PLST PAN POS	1
36	SCW No6x3/8" PLST PAN POS	1
37	WSHR M2,5 SPRF IT STL	2
38	RIVET PLST DOME 3,1Dx4THK	1
39	LABEL HiVOLT40mmSq MAX SA	1
40	FOOT S/A RUBR 8Dx2.5Hmm	2

*per batch

PCB assembly parts list

Item	Description	Qty
1	BARE PCB	1
2	A3000 PCB ASSEMBLY DWG	1*
3	A3000 PCB CIRCUIT DIAGRAM	1*
6	PCB BACK PANEL	1
9	CONR 2W SHUNT 0.1" (FITTED TO LK17-20,24-29)	10
10	SKT IC 24/0.3" NORM (IC7)	1
11	SKT IC 28/0.6" NORM (IC1)	1
12	SKT IC 32/0.6" SUPA (IC14-17)	4
13	SKT IC 40/0.6" NORM	1IC2
15	WIRE 25SWG CPR TIN A/R (X1,X2,X3)	
17	LABEL SERIAL PCB 15x50mm	1
19	RIVET AVDEL 11070312 (SK15)	2
R1	RES 1K0 SMD 5% 0W25 1206	1
R2	RES 1K0 SMD 5% 0W25 1206	1
R3	RES 180R SMD 5% 0W25 1206	1
R4	RES 330R SMD 5% 0W25 1206	1
R5	RES 270R SMD 5% 0W25 1206	1
R6		N/F
R7	RES 180R SMD 5% 0W25 1206	1
R8	RES 100R SMD 5% 0W25 1206	1
R9	RES 22K SMD 5% 0W25 1206	1
R10	RES 4K7 SMD 5% 0W25 1206	1
R11	RES 1K0 SMD 5% 0W25 1206	1
R12	RES 4K7 SMD 5% 0W25 1206	1
R13	RES 4K7 SMD 5% 0W25 1206	1
R14	RES 330R SMD 5% 0W25 1206	1
R15	RES 2K2 SMD 5% 0W25 1206	1
R16-R24	RES 22R SMD 5% 0W25 1206	9
R25-R28	RES 4K7 SMD 5% 0W25 1206	4
R29	RES 1K0 SMD 5% 0W25 1206	1
R30	RES 4K7 SMD 5% 0W25 1206	1
R31	RES 4K7 SMD 5% 0W25 1206	1
R32	RES 10K SMD 5% 0W25 1206	1
R33	RES 10K SMD 5% 0W25 1206	1
R34	RES 330R SMD 5% 0W25 1206	1
R35	RES 330R SMD 5% 0W25 1206	1
R36	RES 1K0 SMD 5% 0W25 1206	1
R37	RES 100K SMD 5% 0W25 1206	1
R38	RES 100K SMD 5% 0W25 1206	1
R39	RES 100K SMD 5% 0W25 1206	1
R40	RES 10K SMD 5% 0W25 1206	1
R41	RES 100K SMD 5% 0W25 1206	1
R42	RES 100K SMD 5% 0W25 1206	1
R43	RES 1K0 SMD 5% 0W25 1206	1
R44	RES 4K7 SMD 5% 0W25 1206	1
R45	RES 5K6 SMD 5% 0W25 1206	1
R46	RES 680R SMD 5% 0W25 1206	1
R47	RES 10R SMD 5% 0W25 1206	1
R48	RES 1K2 SMD 5% 0W25 1206	1
R49-R65	RES 68R SMD 5% 0W25 1206	17
R66	RES 330R SMD 5% 0W25 1206	1
R67-R71	RES 22R SMD 5% 0W25 1206	5
R72-R75	RES 4K7 SMD 5% 0W25 1206	4
R76	RES 5K6 SMD 5% 0W25 1206	1
R77	RES 680R SMD 5% 0W25 1206	1
R78	RES 10R SMD 5% 0W25 1206	1
R79	RES 332R MF 1% 0W25 E96	1
R80	RES 33R SMD 5% 0W25 1206	1
R81	RES 3K3 SMD 5% 0W25 1206	1
R82	RES 22K MF 1% 0W25	1
R83	RES 332R MF 1% 0W25 E96	1
R84	RES 56R SMD 5% 0W25 1206	1
R85	RES 3K3 SMD 5% 0W25 1206	1
R86	RES 22K MF 1% 0W25	1
R87	RES 68R SMD 5% 0W25 1206	1

2Mb RAM upgrade

Item	Description	Qty
1	BARE PCB	1
2	ASSEMBLY DRAWING	1*
3	CIRCUIT DIAGRAM	1*
C1-C8	CPCTR DCPLR 100n AXA 25V	8
C9	CPCTR 47u ALEC 16V RAD	1
C10	CPCTR 47u ALEC 16V RAD	1
IC1-IC8	IC DRAM 256Kx4 120n 20ZIP	8
SK1	CONR 20W SKT 0.1" RA PCB	1
SK2	CONR 20W SKT 0.1" RA PCB	1
SK3	CONR 20W SKT 0.1" RA PCB	1

* per batch

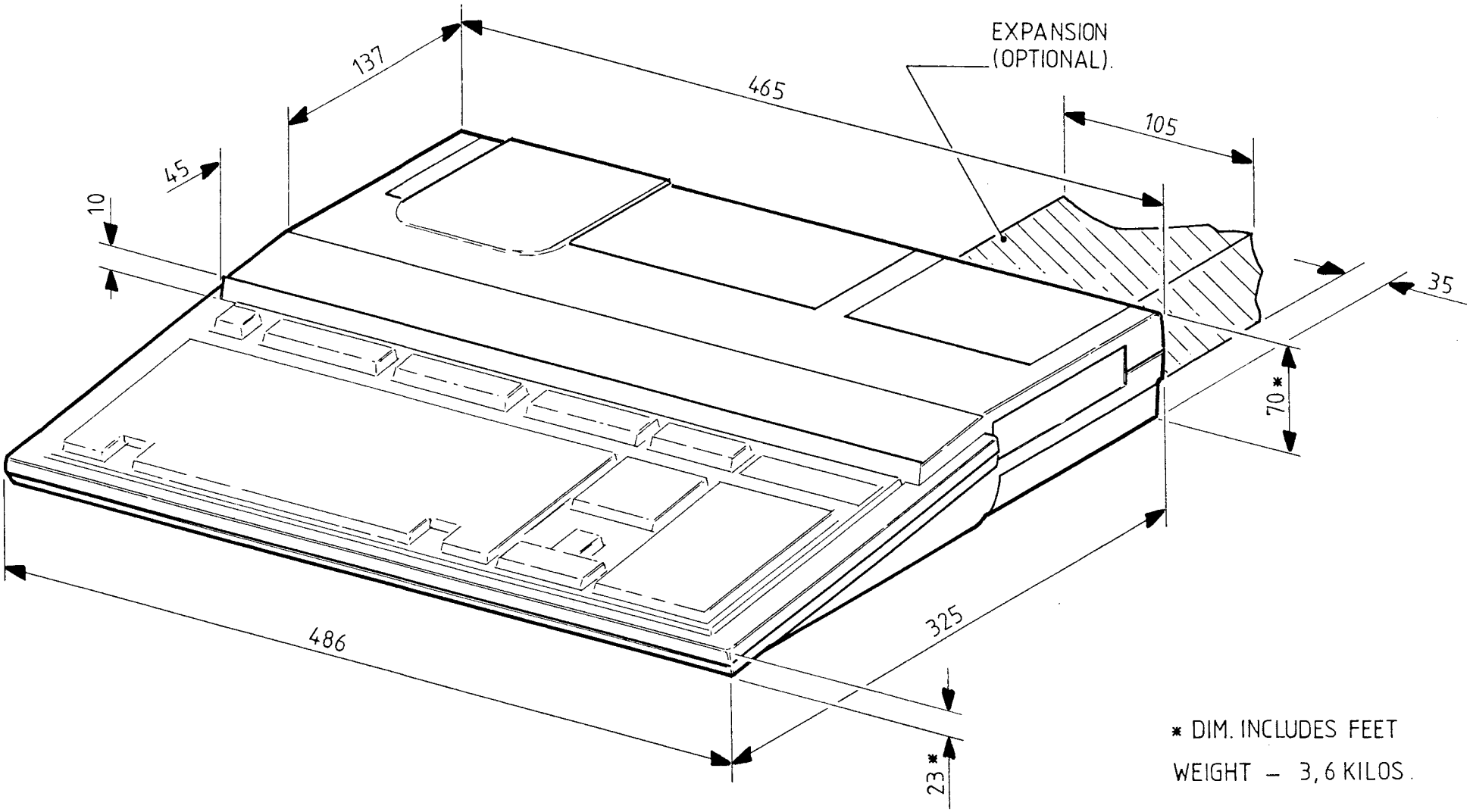
User Port MIDI upgrade

Item	Description	Qty
2	ASSEMBLY DRAWING	1*
3	CIRCUIT DIAGRAM	1*
6	PCB REAR PANEL	1
9	SKT IC 28/0.6" NORM	1IC3
11	RIVET POP DOME 3,2D & THK (USE ON ITEM 6)	2
L1-L18	RES ZERO R 0W25	18
R1	RES 2K2 C/MF 5% 0W25	1
R2	RES 2K2 C/MF 5% 0W25	1
R3	RES 220R C/MF 5% 0W25	1
R4	RES 220R C/MF 5% 0W25	1
R5	RES 220R C/MF 5% 0W25	1
R6	RES 220R C/MF 5% 0W25	1
R7	RES 1K0 C/MF 5% 0W25	1
R8	RES 2K2 C/MF 5% 0W25	1
R9	RES 2K2 C/MF 5% 0W25	1
R10	RES 220R C/MF 5% 0W25	1
R11	RES 10K C/MF 5% 0W25	1
R12	RES 10K C/MF 5% 0W25	1
C1	CPCTR 220u ALEC 16V RAD	1
C2-C8	CPCTR DCPLR 33/47n 0.2"	7
IC1	IC 65C22 VIA CMOS 2MHz	1
IC2	OPTO ISOL 6N138 8/0.3"	1
IC3	ROM {0727,128/9 TBP}	1
IC4	IC 7406 TTL 14/0.3"	1
IC5	IC 2691 UART CMOS 24/0.3"	1
IC6	IC 74HC139 CMOS 16/0.3"	1
D1	DIODE 1N4148 SI	1
LK1-LK4		N/F
SK1	CONR 20W HDR IDC RA 4WALL	1
SK2	CONR 5W SKT DIN RA PCB	1
SK3	CONR 5W SKT DIN RA PCB	1
SK4	CONR 5W SKT DIN RA PCB	1
SK5	CONR 17W WAFR 0.1 23,5mmL	1
SK6	CONR 17W WAFR 0.1 23,5mmL	1

* per batch

Item	Description	Qty
C85	CPCTR CPLT 1n 30V 10%	1
C86	CPCTR CPLT 2n2 30V 10%	1
C87	CPCTR DCPLR 33n SMD 1210	1
C88	CPCTR MPSTR 100n 50V 10%	1
C89	CPCTR TANT 10u 10V 20%	1
C90	CPCTR CPLT 2n2 30V 10%	1
C91	CPCTR CPLT 2n2 30V 10%	1
C92	CPCTR MPSTR 22n 50V 10%	1
C93	CPCTR ALEC 10u 16V RAD	1
C94	CPCTR TANT 10u 10V 20%	1
C95	CPCTR ALEC 47u 16V RAD	1
C96	CPCTR CER 47n 30V 80%	1
C97	CPCTR ALEC 10u 16V RAD	1
C98	CPCTR DCPLR 33n SMD 1210	1
C99	CPCTR DCPLR 33n SMD 1210	1
C100	CPCTR TANT 10u 10V 20%	1
C101		N/F
C102		N/F
C103		N/F
C104		N/F
C105	CPCTR DCPLR 33n SMD 1210	1
C106	CPCTR DCPLR 33n SMD 1210	1
C107	CPCTR CER 47n 30V 80%	1
C108	CPCTR TANT 10u 10V 20%	1
C109	CPCTR ALEC 47u 10V AX	1
C110	CPCTR ALEC 47u 10V AX	1
C111	CPCTR TANT 10u 10V 20%	1
C112	CPCTR ALEC 220u 16V RAD	1
C113	CPCTR DCPLR 33n SMD 1210	1
C114	CPCTR CPLT 10p 30V 2%	1
C115	CPCTR CPLT 33p 30V 2%	1
C116	CPCTR CPLT 2n7 30V 10%	1
C500-C506	CPCTR DCPLR 33n SMD 1210	7
IC1		N/F
IC2	IC KBD CNTRLR {0708,051}	1
IC3	IC 7438 TTL 14/0.3"	1
IC4	IC 74LS145 TTL 16/0.3	1
IC5	IC 74LS145 TTL 16/0.3	1
IC6	IC 8583 RTC RAM 8/0.3"	1
IC7		N/F
IC8	IC 74HCT14 CMOS 14/0.3"	1
IC9	IC 74HC04 CMOS 14/0.3"	1
IC10	IC 74HC74 CMOS 14/0.3"	1
IC11	IC 74LS374 TTL 20/0.3"	1
IC12	IC 74HC138 CMOS 16/0.3"	1
IC13	IC IOC {PLSTC}	1
IC14	RISC OS ROM 1 V2.0	1
IC15	RISC OS ROM 2 V2.0	1
IC16	RISC OS ROM 3 V2.0	1
IC17	RISC OS ROM 4 V2.0	1
IC18	IC 74HC574 CMOS 20.0.3"	1
IC19	IC 74HC574 CMOS 20.0.3"	1
IC20-IC27	IC DRAM 256Kx4 120n 20ZIP	8
IC28	IC 74HC139 CMOS 16/0.3"	1
IC29	IC 74HC573 CMOS 20/0.3"	1
IC30	IC 74HC573 CMOS 20/0.3"	1
IC31	IC 74HC573 CMOS 20/0.3"	1
IC32	IC LM386 AUDIO AMP	1
IC33	IC 74HC139 CMOS 16/0.3"	1
IC34	IC 74HC00 CMOS 14/0.3"	1
IC35	IC 7406 TTL 14/0.3"	1
	IC 7416 TTL 14/0.3" (OPTION)	
IC36	IC 1772 FDC 28/0.6"	1
IC37	IC ARM {2um PLSTC}	1
IC38	IC LM386 AUDIO AMP	1
IC39	IC LM324 QUAD OP AMP	1
IC40	IC 74AC86 CMOS 14/0.3"	1
IC41	IC VIDC 1A {PLSTC}	1
IC42	IC 74HCT573 CMOS 20/0.3"	1
IC43	IC 74HC573 CMOS 20/0.3"	1
IC44	IC MEMC 1A {PLSTC-8MHz}	1
IC45	IC 74HCT573 CMOS 20/0.3"	1
IC46	IC 74HC573 CMOS 20/0.3"	1
IC47	IC 74HC04 CMOS 14/0.3"	1

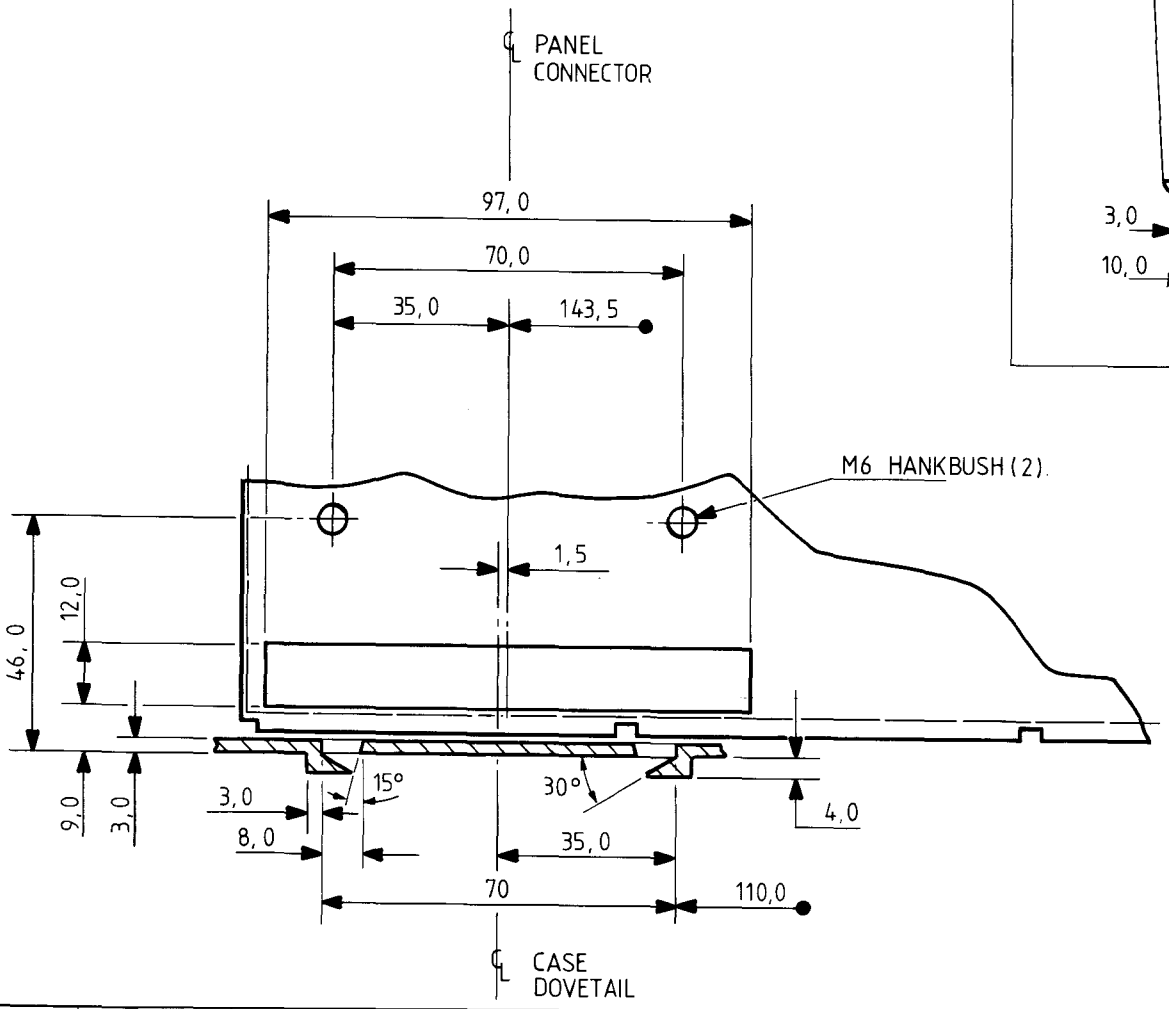
Item	Description	Qty
Q1	TRANS BC239 NPN 0.2"P LDS	1
Q2-Q10	TRANS 2N3906 PNP .2"P LDS	9
Q11	TRANS BC239 NPN 0.2"P LDS	1
Q12	TRANS BC239 NPN 0.2"P LDS	1
D1		N/F
D2	DIODE SI 1N4005 600V 1A	1
D3-D16	DIODE SI 1N4148	14
B1	BAT NICAD 1V2 280mAH PCB	1
L1-	RES ZERO-OHM 0W25 (0.6"ptch)	14
L14	WIRE 22SWG TIN (OPTION)	
L15		N/F
L16	CHOKE RF FE BEAD	1
L17	CHOKE RF FE BEAD	1
L18	CHOKE RF 2u2H AX Q=30	1
L19	COIL RF 33uH AX Q=45	1
L20	CHOKE RF FE BEAD	1
L21	CHOKE RF FE BEAD	1
LK1-LK16		N/F
LK17	CONR 2W WAFR 0.1" ST PCB	1
LK18	CONR 2W WAFR 0.1" ST PCB	1
LK19	CONR 3W WAFR 0.1" ST PCB	1
LK20	CONR 3W WAFR 0.1" ST PCB	1
LK21		N/F
LK22	CONR 2W WAFR 0.1" ST LK	2
LK23	CONR 2W WAFR 0.1" ST LK	2
LK24	CONR 3W WAFR 0.1" ST PCB	1
LK25	CONR 2W WAFR 0.1" ST PCB	1
LK26	CONR 2W WAFR 0.1" ST PCB	1
LK27	CONR 2W WAFR 0.1" ST PCB	1
LK28	CONR 2W WAFR 0.1" ST PCB	1
LK29	CONR 2W WAFR 0.1" ST PCB	1
LK30	CONR 2W WAFR 0.1" ST PCB	1
LK31	CONR 2W WAFR 0.1" ST PCB	1
PL1	EARTH STRAP {PCB/PSU}	1
PL2	CONRD 9W PLG RAPCB+RFI+LK	1
PL3	FSTN TAB 6,3mmx0,8 ST PCB	1
PL4	FSTN TAB 6,3mmx0,8 ST PCB	1
PL5		N/F
PL6	CONR 34W BOX IDC LP ST	1
SK1	CONR 9W MINDIN RA PCB	1
SK2	CONR 5W SKT DIN RA PCB	1
SK3	CONR 17W SKT 0.1" PCB	1
SK4	CONR 17W SKT 0.1" PCB	1
SK5	CONR 5W SKT HSNG 0.1" PCB	1
SK6	CONR 20W 0.1" FLXPCB SKT	1
SK7	CONR 20W 0.1" FLXPCB SKT	1
SK8	CONR 5W SKT 0.1" PCB	1
SK9	CONR 5W SKT 0.1" PCB	1
SK10	CONRD 25W SKT RAPCB+RFI+L	1
SK11	CONR 17W SKT 0.1" PCB	1
SK12	CONR JKSKT 3W 3,5mm RAPCB	1
SK13	CONR PHONO SKT RA PCB	1
SK14	CONRD 9W SKT RAPCB+RFI+LK	1
SK15	CONR 64W SKT RA AC PCB	1
SK16	CONR 20W WAFR 0.1 ST 10mm	3
SW1	SW 2P MOM CO P/B RA PCB	1
X1	XTAL 1.8432MHz HC18	1
X2	XTAL 32.768KHz CC 0.05"	1
X3	XTAL 24.00MHz HC18	1

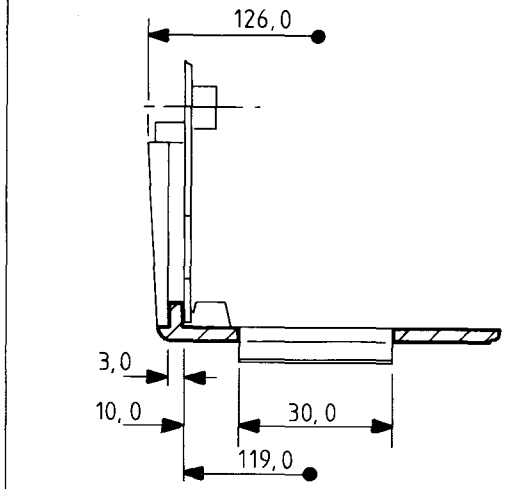


* DIM. INCLUDES FEET

WEIGHT – 3,6 KILOS.

A3	DRG. No. 0280, 365/	FIRST USED ON	THIRD ANGLE PROJECTION	IF IN DOUBT ASK	DO NOT SCALE





ISS	DATE	DESC. OF CHANGE	DRN	CHK
1	3/7/89	AMR2329	IRS	
B	27/6/89	REDRAWN	IRS	

SCALE	1:1	ALL DIMENSIONS IN mm UNLESS OTHERWISE STATED
MATL		
FINISH		

TITLE

A3000 - EXTERNAL EXPANSION FIXING